

A

Sir:

Transmitted herewith for filing is the Patent Application of:

Inventor: MOU-SHIUNG LIN

For: A MULTIPLE SELECTABLE FUNCTION INTEGRATED CIRCUIT MODULE

JCS30 U.S. PTO  
09/246303



Enclosed are:

- ☒ 10 sheets of drawing(s) - formal.  
☐ An assignment of the invention to  
☐ An associate power of attorney

☒ Small Entity Form

The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	OTHER THAN A SMALL ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE
BASIC FEE				\$ 760.
TOTAL CLAIMS	51 -20=	31	x 18 =	\$ 558.
INDEP CLAIMS	7 -3=	4	x 78 =	\$ 312.
MULTIPLE DEPENDENT CLAIM PRESENTED			+ 260 =	
			SUB TOTAL	\$ 1,630.
			ASSIGNMENT	
			TOTAL	\$ 1,630.

☒ Please charge my Deposit Account No. 19-0033 in the amount of \$ 1,630. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 19-0033. A duplicate copy of this sheet is enclosed.

- ☒ Any additional filing fees required under 37 CFR \$1.16.  
☒ Any patent application processing fees under 37 CFR \$1.17.

Respectfully submitted,

STEPHEN B. ACKERMAN, REG. NO. 37,761

EXPRESS MAIL CERTIFICATE

EXPRESS MAIL NO. EJ548 799243US

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: The Commissioner of Patents & Trademarks, Washington, D.C. 20231. Applicant and/or Attorney requests the date of deposit as the filing date.

Date of Deposit

Feb. 8, 1998

Signature

Reg # 37,761

Date

2/8/99

# A MULTIPLE SELECTABLE FUNCTION INTEGRATED CIRCUIT MODULE

## Background of the Invention Field of the Invention

### 5 Related Patent Applications

This invention is related to the U. S. Patent Application having the attorney's docket number **MSLin98-004**, serial number \_\_\_\_\_, filing date \_\_\_\_\_.

10

### Field of the Invention

This invention is related to integrated circuits. More particularly, this invention relates to multiple function integrated circuit chips such as Dynamic Random Access Memories (DRAM) having function selection through wiring connections on a second level substrate onto which an integrated circuit chip is mounted.

15

### Background of the Related Art

The structure of a DRAM is well known in the art. Usually a DRAM chip is configured to be organized as a X1 (by 1), X4 (by 4), X8 (by 8), or X16 (by 16)

20

package by selective destruction of fuses internal to the DRAM chip and by selectively connecting the data input/output pads to pins on a package. The unused pins are not connected to the input/output pads of the undesired or unused data transfer pads. Refer now to Fig. 1 for a schematic drawing of the structure of a DRAM integrated circuit showing the input/output selection function. A DRAM array **100** has multiple banks of arrays of DRAM cells. Address signals are applied to the address I/O's **105** and decoded within column address and row address decoders to select DRAM cells within the DRAM array **100**.

Control and timing signals **120** are applied to the control logic and timing generator **115** to provide the necessary control and timing functions for the DRAM array **100**.

Upon applying an address to the DRAM array **100**, digital data is transferred to or from the DRAM array **100** by the internal data bus **110**. The internal data bus **110** is connected between the sense amplifier and I/O bus on each memory bank. The internal data bus **110** may conceptually have a connection for each column of one memory bank, but usually is the maximum data bit width configuration of the DRAM integrated circuit.

The internal data bus **110** is connected to the input/output selector **125**. The input/output selector **115** determines the interconnections between the

input/output buffers **130** and the internal data bus **110**. The selection pins **140** of the input/output selector **125** are connected to the selection networks formed of the resistors **145a**, **145b**, and **145c** and the fuses **150a**, **150b**, and **150c**. A logical one state is applied to the selection pins **140**, if a fuse **150a**, **150b**, and **150c** is opened. A logical zero state is applied to the selection pins **140**, if a fuse **150a**, **150b**, and **150c** remains intact. The logical states applied to the selection pins **140** determine which connections on the internal data bus **110** are connected to which of the input/output buffers **130**. While, as shown, the selector circuits will draw unacceptable amounts of standby current, it is presented here for illustration. Other techniques known in the art are used to form the selection networks.

The input/output buffers **130** are connected to the pads **135**. The fuses **150a**, **150b**, and **150c** of the selection network are opened either as a masking during a final metalization or personalization by blowing the fuses **150a**, **150b**, and **150c** with highly intense laser light prior to separation of a wafer containing the DRAM integrated assembly into DRAM modules.

Those input/output pads **135** not used for a configuration are not connected to the module connections during the next level assembly. The fused configuration selection forces the maintenance of inventory of the DRAM die for each desired configuration increasing the difficulty in planning of production of DRAM wafers.

While the structure of the prior art as shown in Fig. 1 is described for a DRAM, other integrated circuit functions such as computational processors (microprocessors, microcontrollers, digital signal processors, etc.),

5 programmable memory, and programmable logic arrays employ metal masking or fuse destruction at the wafer level, and making or omitting connections during attachment of the functional integrated circuit die to a next level package assembly. This complicates the semiconductor processing in that extra masking steps are required for mask programming of desired functions of the functional  
10 integrated circuit die. Each function desired requires a unique mask for the selection process, further complicating the semiconductor process. Additionally, fuse destruction adds an extra step in the processing of the functional integrated circuit die.

15 Fig. 2 shows a process for forming integrated circuit modules. The process begins with the formation **200** of the integrated circuit chip on a semiconductor wafer. The semiconductor process **210** forms the collection of transistors that are the electronic circuits on the semiconductor wafer. The electronic circuits are interconnected by metalization and are also connected to  
20 input/output pads by the metalization placed on the surface of the semiconductor wafer. During the metalization, optional functions may be personalized to select optional functions. In the case of the DRAM of Fig. 1, the fuses **150a**, **150b**, and **150c** are either opened or held intact during this process to select the desired

input/output organization options. An alternative to selecting the desired input/output organization options of the DRAM of Fig. 1 is exposing the metalization on the surface of the semiconductor substrate that forms the fuses **150a**, **150b**, and **150c** to intense laser light to destroy the appropriate fuses **150a**, **150b**, and **150c**.

The steps of formation of the integrated circuit chip is common for all the desired selectable functions until the metalization to select the desired functions. The integrated circuit chips then becomes a custom design. Equally, the integrated circuit chip has a common design until the destruction of fuses to create the custom personalization that selects each desired function of the integrated circuit chip.

The semiconductor wafer is placed on a test system and each integrated circuit chip is tested **220** for functionality. The functioning chips are denoted as functional die. The semiconductor wafer is then diced **220** and the functional die are separated for further assembly **225** in a first level or module package. The selection or omission of connections between the functional integrated circuit die and the first level package is a custom design particular to each combination of desired functions.

The input/output pads of the desired functions of the functional die are connected by a method such as wire bonding or tape automated bonding to the

pins of the first level package. The input/output pads of the undesired function are omitted during the wire bonding or tape automated bonding. The package is tested **230** and inventoried **235** for further assembly.

5           The assembly **205** of the second level package begins by forming **240** the substrate of the second level assembly. Multiple layers substrate are formed having interconnection metalization that connects the packaged and tested die to external circuitry that is present either on the second level package or elsewhere within the electronic system. The multiple layers are assembled to form the  
10   substrate of the second level assembly.

          A solder mask is placed **245** on the second level assembly and a solder paste is placed **250** at all connection points of the packaged and tested die. The packaged and tested die is attached **255** to the second level assembly. In a  
15   surface mounted packaging system, the solder paste is melted and the pins of the packaged and tested die fused to the metalization of the second level assembly. The remaining processing of the second level assembly is completed **260**.

20           For integrated circuit modules having multiple functions, the metalization of the second level assembly must be customized. Again, this increases the number of assembly types required to be inventoried.

U.S. Patent 5,360,992 (Lowery et al.) discloses a semiconductor package which allows pinouts and bond options to be customized after encasement of a semiconductor die. The semiconductor package has two assemblies in a first embodiment and an optional third assembly in a second embodiment.

5

A first assembly comprises a semiconductor die encased in plastic, ceramic, or other suitable material. All available bond options (bond pads) are routed to the exterior portion of the package by a first assembly frame. Portions of the first assembly frame are exterior to the encasement and terminate in exterior pad portions that can be conductively bonded to.

10

A second assembly of the invention comprises a second assembly frame that provides a means of input/output (I/O) between the packaged die and a next level of assembly onto which it is installed. The second assembly frame comprises conductive paths to which the exterior pad portions are connected, the first assembly being conductively mounted to the second assembly thereby.

15

With the two-piece embodiment of the invention, the frame of the second assembly determines the pinouts (the pin numbers associated with each of the signals of the device) of the various signals of the die contained within the first assembly.

20

The optional third assembly, which, if used, is interposed between the first and second assemblies, comprises means for "keying" the exterior pad portion



desired locations or the second assembly frame. The assembly can comprise at least two different forms.

In the first form, the third assembly is a nonconductive membrane having  
5 voids therethrough, conductive paths of the second assembly are located in an  
"X" direction, while the exterior pad portions of first assembly of this form are  
bars extending in a "Y" direction. By selectively placing the voids in the  
membrane, the pads of the first assembly can either be connected with the  
conductive paths of the second assembly or isolated from the conductive paths if  
10 no void is formed. Using the X-Y arrangement, any of the bond options can be  
connected with any of the pinouts. Connecting is accomplished by coating the  
bars with a conductive material and interposing the insulative membrane  
between the first and second assemblies. The conductive material fills the voids,  
thereby passing signals between the first and second assemblies.

15  
In the second form, the third assembly comprises a flex circuit as used  
with tape automated bonding. The second assembly has a single design, and  
the layout of the flex circuit determines the pinouts and options of the  
semiconductor device. The flex circuit is conductively mounted to the first and  
20 second assemblies in a fashion consistent with tape automated bonding (TAB)  
technology, for instance with solder, or by some other means such as conductive  
epoxy.

U.S. Patent 5,737,767 (Agrawal et al.) teaches a random access memory (RAM) array with a reconfigurable bit width or word width. In one embodiment, a reconfigurable x-y RAM array is provided which includes a memory array comprised of a plurality of RAM cell columns. The RAM cell columns are

5 organized into a number of groups where the number of groups corresponds to the bit width of the memory. Each group contains an equal number of columns so that the number of columns in a group multi number of groups equals the total number of array. The number of columns in a group is reconfigurable according to the present invention. Thus, when the number of columns in a group is

10 smaller, the number of groups is larger and when the number of columns in a larger, the number of groups is smaller. Thus, the bit width of the memory is reconfigurable by modifying the number of columns in a group, since the bit memory corresponds to the number of groups.

15 To access a word stored in the array, The RAM decodes an address and selects one bit from each column group. Thus, the word size stored by the RAM is determined by the number of columns groups configured in the array.

Agrawal et al. provides multiplexer (mux) logic coupled to each column.

20 Column select logic decodes a memory address and provides select signals corresponding to the address to the mux logic. The mux selects a particular column in the group to be accessed and outputs a column bit signal indicative of the memory state of the selected column.

Column configuration logic is coupled to the mux logic and combines the mux outputs into memory bit signals. The mux outputs combined by the column configuration logic determine the size of the column groups from which a memory bit signal is selected. The column configuration logic may be placed in different modes to configure different column group sizes and thus to reconfigure the bit width of the memory. The column select logic is responsive to the configuration mode and decodes the address for the appropriate column group size.

## Summary of the Invention

An object of this invention is to provide integrated circuit modules having common known good integrated circuit die. Selectable functions of the known good integrated circuit die are chosen during packaging of the known good integrated circuit die. Such selectable functions allow a reduction of the variety of integrated circuit components during manufacturing and assembly. This provides a method to reduce the required inventory of integrated circuit components at integrated circuit manufacturers, distributors, and integrated circuit users.

Another object of this invention is a method of assembly of integrated circuit modules to choose selectable functions of known good integrated circuit die to be mounted in the integrated circuit modules.

Further, another object of this invention is to eliminate a first level of packaging by using a wafer level processing to provide all possible connections from a known good integrated circuit die. The wafer level processing of all possible connections allow gang-bonding of desired functions on a known good integrated circuit die at no additional processing cost.

The integrated circuit module has an integrated circuit known good die to be mounted to the module. The integrated circuit known good die has multiple selectable input functions, multiple selectable output functions, common functions, a function selector, all are interconnected and connected to input/output pads. The integrated circuit known good die is mounted to a second level substrate. The second level substrate has wiring connections to the input/output pads of the integrated circuit known good die that select desired input functions and output functions. Further, the wiring connections on the second level substrate provide signal paths to transfer signals to the desired input function and signals from the desired output function, and signals to and from the common functions. Also, the wiring connections form connections between the input/output pads and external circuitry. To select the desired input functions and the desired output functions, appropriate logic states are applied to input/output pads connected to function selector to configure a functional operation of the integrated circuit module. The second module substrate has

connector pins to provide physical and electrical connections between the external circuitry and the wiring connections on the second level substrate.

The integrated circuit known good die may be a DRAM integrated circuit die. The DRAM integrated circuit die has a plurality of selectable input/output organizations. Each of the selectable input/output organizations is selected as one of the logic states to the function selector and connections from the second level substrate to unused input/output function connected to input/output pads of the DRAM are omitted from the second level substrate.

The integrated circuit known good die may be a common computational processor (a microprocessor, a microcontroller, a digital signal process, etc.).

The common computational processor has selectable input functions and selectable output functions that include analog-to-digital converters, digital-to-analog converters, general purpose word-width input/output buses, standard compliant serial interfaces, interfaces to host processors of a system, control signal inputs and outputs, timer/counter inputs and outputs, computer operating properly signals, and interrupt signals.

In one implementation of the integrated circuit module, the input/output pads of the known good die have solder bumps, which are arranged as a ball grid array. The selectable input functions and the selectable output functions are chosen by creating or omitting voids in a solder mask on the second level

substrate during assembly. The desired connections are then made to the second level substrate and the undesired connections are omitted.

The method to form an integrated circuit module begins by forming an integrated circuit die having multiple selectable input functions, multiple selectable output functions, common functions, and a selector function. The integrated circuit die is created by forming electronic components on a surface of a semiconductor wafer to form the multiple selectable input functions, the multiple selectable output functions, common functions, the selector function.

Redistribution metallurgy is then formed on the surface of the semiconductor wafer to form input/output pads connected to the multiple selectable input functions, the multiple selectable output functions, the common functions, the selector functions. The integrated circuit die is then tested to determine functional integrated circuits die. The semiconductor wafer is then diced to separate integrated circuit die are then burned-in, tested to find the known good integrated circuit die. The known good integrated circuit die are then sorted and inventoried.

The second level substrate is created by forming metal interconnections on multiple layers of the second level substrate, and laminating of the multiple layers of the second level substrate. The integrated circuit module is then assembled by applying a solder mask to a component level of said second level substrate. The solder mask is applied to the second level substrate so as to

have voids to expose the input/output pads of the common functions, desired functions of the multiple selectable input functions and the multiple selectable output functions, and the input/output pads that select the desired functions with input and output functions. The solder mask will have the voids omitted to  
5 eliminate the connections of the non-desired functions of the multiple selectable input functions, the multiple selectable output functions, the selector function by coating the input/output pads of the non-desired functions. A solder paste is deposited on the input/output pads exposed by the solder mask. The known good integrated circuit die is then placed and secured to the component level of  
10 the second level substrate. The method is then completed with final assembly and test of the integrated circuit module.

### Brief Description of the Drawings

Fig. 1 is a schematic diagram of a DRAM illustrating the configuring  
15 circuitry of the prior art.

Fig. 2 is a flow chart illustrating the method of assembly of an integrated circuit chip on a second level assembly of the prior art.

20 Fig. 3 is a diagram of an integrated circuit module illustrating the configurability of a known good integrated circuit die having multiple selectable functions of this invention.

Fig. 4 is a schematic diagram of a DRAM illustrating the configuring circuitry of this invention.

5 Figs. 5a – 5e are diagrams of an area array of input/output pads of a DRAM module illustrating the configurations of the data input/output pins of this invention

Fig. 6 is a schematic diagram of a multiple selectable function computational processor illustrating the configuration structure of this invention.

10 Fig. 7 is a diagram of a flow chart illustrating the method of assembly of a known good integrated circuit die on a second level assembly of this invention.

15 Fig. 8 is a diagram of an integrated circuit module illustrating the configurability of multiple a known good integrated circuit dies having multiple selectable functions of this invention.

### Detailed Description of the Invention

20 For a description of a general description of a general embodiment of this invention, refer now to Fig. 3. A multiple selectable function integrated circuit die **300** has a plurality of selectable input functions **306** and selectable output functions **308** and common functions **304**. The selectable input functions **306** are circuits that implement such functions as interface standard receivers, analog-to-



digital converters, and address and control decoders. The selectable output functions **308** are circuits that implement such functions as interface standard drivers, digital-to-analog converters, address drivers, data drivers, control drivers, and timing signal drivers. The common functions **304** are circuits that implement

5 such functions as DRAM array address and support functions, SRAM array address and support functions, non-volatile memory array address and support functions, computational processor circuitry such as arithmetic logic units and multiply accumulate function, program decoder circuits, timing circuits, and address generation. A select function **310** is connected to the selectable input

10 functions **306**, the selectable output functions **308**, and the common functions **304** by the internal input bus **374**, the internal output bus **372**, and the internal common bus **376**. The computational processor may be configured as a microprocessor, a microcontroller, a digital signal processor, or other complex logic function.

15 The select function **310**, is based on the logic states of the select signals **378**, the common select signals **380**, output select signals **382**, the interconnections between the internal input bus **374**, the internal output bus **372**, and the internal common bus **376**. Any of the selectable input functions **306**,

20 selectable output functions **308**, and common functions **304** that are not to be configured are effectively disabled and disconnected from those that being configured for a given configuration of the integrated circuit module.

Not shown in the connections to power supply voltage sources and to the ground reference points. These connections are required for the functioning of the known good integrated circuit die **300** and in fact may be connected or disconnected from the selectable input functions **306** or the selectable output functions **308** as part of the selection of these functions.

The common input and the common output signals **386** and **388** that are common to all configurations of the integrated circuit module are introduced to the common input module connectors **336** and are received from the common output module connectors **336**. The common input module connectors **336** have internal module wiring **390** connected to the common input module pads **334**. The common input module pads **334** are connected **332** in a predetermined fashion to the common input pads **330** on the integrated circuit die **300**. Conventionally, input module pads **334** are connected to the input pads **330** as wirebonds, tape automated bonds, and solder bumps of ball grid array. The common output module connectors **384** have internal module wiring **398** connected to the common output module pads **340**. The common output module pads **340** are connected **342** in a predetermined fashion to the common output pads **338** on the integrated circuit die **300**. Conventionally, output module pads **340** are connected to the output pads **338** as wirebonds, tape automated bonds, and solder bumps of ball grid array. The common input signals **386** and the common output signals **388** are typically, but not exclusively, timing control, and test stimulus signals.

The selectable input function signals **312** are introduced through the selectable input function module connectors **320**. The selectable input function module connectors **320** are attached to the internal module wiring **392**, which is connected to the selectable input module pads **316**. The selectable input module pads **316** that will have desired selectable input function signals **312** will be connected **318** to the selectable input/output pads **314** on the integrated circuit die **300**. The undesired selectable input function signals will be omitted from the connections **318** between the selectable input module pads **316** and the selectable input pads **314**. As described above, the connections **318** may be wire bonds, tape automated bonds, or solder bumps of a ball grid array.

Similarly, the selectable output function signals **394** are transferred to external circuitry connected to the integrated circuit module on a second level of packaging through the selectable output function connectors **328**. The selectable output function connectors **328** are attached to the integrated circuit module wiring **396** to the selectable output function module pads **324**. The desired selectable output function signals **394** are transferred from the desired output function **308** to the output pads **322** on the integrated circuit die **300**. The desired output pads **322** are connected to the corresponding selectable output function module pads **324** and thus to the selectable output function module connectors **328**. The undesired output function signals **394** on the output pads

**322** are omitted from connection to the selectable output function module pads **324**.

The input function select signal **378**, the common function select signals **380**, and the output function select signals **382** are transferred from external circuitry respectively through the input option select module connectors **348**, the common option select module connectors **356**, and the output option select module connectors **364**. The input option select module connectors **348**, the common option select module connectors **356** and output option select module connectors **364** are respectively connected through module interconnecting wire to the input option select module pads **354**, the common option select module pads **344**, and the output option select module pads **362**.

Generally, the input function select signals **378**, the common function select signals **380**, and the output function select signals **382** are logic states established by either the power supply voltage source **Vdd** for a logic state of 1 or a ground reference voltage **GND** for a logic state of 0. To establish one logic state, the input/output pads **342**, **350**, **358** of the integrated circuit die **300** are connected appropriately **346**, **352**, **360** to the input option select module pads **354**, the common option select module pads **344**, and the output option select module pads **362**. Conversely, to establish the second logic state, the input/output pads **342**, **350**, **358** of the integrated circuit die **300** are appropriately omitted from the connections **346**, **352**, **360** to the input option select module

pads **354**, the common option select module pads **344** and the output option select module pads **362**.

One technique for implementing the selection of the multiple selectable functions of the integrated circuit die **300** is to place the input/output pads **314**, **322**, **330**, **338**, **342**, **350**, **358** as an array of connecting pads on the surface of the known good integrated circuit die **300**. A solder bump is applied to each of the input/output pads **314**, **322**, **330**, **338**, **342**, **350**, **358** in a structure of a ball grid array. By connecting or omitting connections to desired input/output pads **314**, **322**, **330**, **338**, **342**, **350**, **358** of the integrated circuit die **300**, the desired functions of the multiple selectable input functions are "gang-bonded" to the module pads **316**, **324**, **334**, **340**, **344**, **354**, **362**. Since the formation of the input/output pads **314**, **322**, **330**, **338**, **342**, **350**, **358** is inherent in the processing of the wafer containing the multiple selectable function integrated circuit die **300**, there is no additional cost in forming the multiple selectable function integrated circuit die **300**. However, since only one design of the multiple selectable function integrated circuit die **300** is maintained, inventory is simplified and costs reduced.

Refer now to Fig. 4 for an implementation of an embodiment of this invention as a DRAM having multiple input/output data width configurations. The structure and function of the DRAM array **100** is as described in Fig. 1. The internal data bus **110** is connected to the input/output pad selector **425**. The data

bus width of the internal data bus **110** is at least the width of the widest data bit width configuration of input/output data bus **455**. The input functions **306** and the output function **308** of Fig. 3 are combined in this embodiment as the data input/output functions **430**, **440**, and **450**.

5

Data is received from or transferred to the DRAM module through the data connections **435**, **445**, and **455**. The data connections **435**, **445**, and **455** are attached to each of the data input/output functions **430**, **440**, and **450**. It should be noted that while each data input/output function **430**, **440**, and **450** have effective different functions, each data input/output function **430**, **440**, and **450** may share one or more of the data connections **435**, **445**, and **455**. In this case, the data input/output functions **430**, **440**, and **450** establish the data bit width configurations and data connections, such as **DQ0**, are shared by all the data input/output functions.

15

Each data connection **DQ0**, **DQ1**, ..., **DQn** is connected to the input of a receiver **480** and the output of a driver **470**. The output of the receiver **480** is the input of the demultiplexer **475**. Each output of the demultiplexer **475** is connected to the input/output selector **425** and through the input/output selector **425** to the internal data bus **110**. The demultiplexer **475** collects singularly, a number of data bits equivalent to the number of bits for the internal data bus **110**, and transfers them through the input/output selector **425**.

20

The internal data bus **110** is connected to the inputs of the multiplexer **465**. The output of the multiplexer **465** is the input of the driver **470**. The output of the driver **470** is connected to one of the data connections **DQ0**, **DQ1**, ..., **DQn**. The multiplexer **465** collects a number of data bits from internal data bus **110** through the input/output selector **425** and serialize these data bits for transfer to the one data connection.

Each of the data input/output functions **430**, **440**, and **450** is comprised of at least one set of the receivers **480**, drivers **470**, multiplexers **465**, and demultiplexers **475** connected to one of the data connections **DQ0**, **DQ1**, ..., **DQn**. This allows the configurations of the input/output data buses **435**, **445**, and **455** to be varied as desired. Thus, a single DRAM array design can be configured with any desired bit data width.

The input/output selector **425** selects which of the input/output functions **430**, **440**, and **450** that are to be configured within a package. The select inputs **460** of the input/output selector **425** provide the appropriate logic states to select the desired input/output configuration or which of the input/output functions **430**, **440**, and **450** are to be implemented. The select inputs **460** are connected to the option decoder **420**. The option decoder **420** is connected to the option receivers **425** which, in turn, are connected to the option select connections **410**.

The DRAM integrated circuit die is processed and tested as described above and the known good die are inventoried. Mounting the known good DRAM die on a second level package such as a "chip-on-chip" structure, a ceramic module, a plastic package, a fiberglass reinforced plastic printed circuit card, or an insulator coated metal selects the desired optional configuration for the DRAM module.

Refer to Figs. 5a-e to discuss an implementation of a DRAM module of this invention as explained in Fig. 4. The known good DRAM die of Fig. 4 has its input/output connections implemented as an array **505** of solder bumps on the surface **500** of the known good DRAM die. The selectable data input/output connections **510** and the option select connections **515** are placed conveniently on the surface of the known good DRAM die. In this instance, it is an area of three columns and six rows.

This implementation as shown is for a DRAM having optional organization X1 (by one), X4 (by four), X8 (by eight), and X16 (by 16). That is there are four input/output functions requiring two option select connections **Op1** and **Op2**. The X1 option activates only the input/output function connected to the selectable data input/output connection **DQ0**. The X4 option activates the input/output functions connected to the selectable data input/output connections **DQ0**, **DQ1**, **DQ2**, and **DQ3**. The X8 option activates the input/output functions connected to the selectable data input/output connections **DQ0**, **DQ1**, ..., and **DQ8**. And



finally, the X16 option activates the input/output functions connected to the selectable data input/output connections **DQ0**, **DQ1**, ..., and **DQ15**,.

Refer now to Figs. 5b-5e for an example of the implementation of the

5     **DRAM** of this invention. Fig. 5b illustrates the implementation of the X1 organization. In this option, the option select connections **515** are made between the known good **DRAM** die and the second level package to connect to the necessary logic states to activate the X1 option. The **DQ0** input/output connection of the selectable data input/output connections **520** is made to the  
10    second level package for transfer of digital signals. The remaining selectable data input/output connections **DQ1**, **DQ2**, ..., **DQ15 520** are masked and the solder balls are not allowed to connect to the interconnecting wiring of the second level substrate.

15     Fig. 5c is a X4 organization. In this option, the input/output function is selected by the option select connection **OP1** being connected to the second level package to place the appropriate logic states at the option desired. The option select connection **OP2** is omitted from being made. The selectable data input/output connections **DQ0**, **DQ4**, **DQ8**, and **DQ12** of the input/output  
20    connections **520** are connected to the second level package. The remaining selectable data input/output connections **DQ1**, **DQ2**, **DQ3**, **DQ5**, **DQ6**, **DQ7**, **DQ9**, **DQ10**, **DQ11**, **DQ13**, **DQ14**, and **DQ15** are masked and those connections are omitted.

Fig. 5d is a X8 organization. In this option, the input/output function is selected by connecting the option select connection **OP2** and omitting the connection of the option select connection **Op1** from the second level package to place the appropriate logic state at the option decoder. The selectable data input/output connections **DQ0, DQ2, DQ4, DQ6, DQ8, DQ10, DQ12, and DQ14** are affixed to the second level package and the selectable data input/output connections **DQ1, DQ3, DQ5, DQ7, DQ9, DQ11, DQ13 and DQ15** are omitted from the second level package.

The X16 option of the known good DRAM die is shown in Fig. 5e. The X16 option is selected by omitting the option select connections **Op1** and **OP2** from the second level package to place the appropriate logic state at the option decoder. All of the selectable data input/output connections **520** are joined to the second level package.

The wiring connections of the second level package onto which the known good DRAM die is mounted can have those wiring tracks to implement all options. The masking stage of the module assembly and the placement of the solder paste determine the option implementation of the DRAM module. Alternately, the interconnection pads that will accept the selectable data input/output connections **520** may be omitted and any unnecessary wiring tracks on the second level package may be omitted. This allows routing of wiring tracks

of the external circuitry on the second level module to change common computational die to selectable function computational die.

A second implementation of the embodiment of this invention is shown in

- 5 Fig. 6. A digital computational processor module has selectable functions to a common computational die **600** to be configured during mounting to a second level package according to desired optional functions. The optional function configures the common computational die as a general-purpose microprocessor, a special function microprocessor, a microcontroller, or a digital signal processor.
- 10 The common computational die **600** has selectable input functions and selectable output functions **605** that include analog-to-digital converters, digital-to-analog converters, general purpose word-width input/output buses, standard compliant serial interfaces, interfaces to host processors of a system, control signal inputs and outputs, timer/counter inputs and outputs, computer operating
- 15 properly signals, and interrupt signals. The selectable function computational die has common input functions and common output functions **615** such as a test interface to provide test stimuli and response for the digital computational module. Other selectable input and output functions **635** will be the address, data, and control functions to interface to external memory array.

20

The internal structure of the selectable function computational die **600** includes certain functions of the computational processor **620**. Common functions are functions like program and control decoder logic **621** and address

generation logic **622**. The selectable functions are the data arithmetic/logic unit **623** and the digital signal processing multiply accumulate unit **624**. Other internal selectable functions **625** are the internal program and data memory and the internal timing circuits. The selectable input and output functions **605**, **635**, the common input and output functions **615**, the internal selectable functions **625**, and the computational processor **620** are interconnected with the data and control bus **630**.

The option select signals **640** provide the appropriate logic states to function select circuit **610** to determine the desired functions of selectable function computational die **600**. The function select circuit is connected to the selectable input and output functions **605** and **635**, the internal selectable functions **625**, and the selectable functions of the computational processor **620** through the selector bus **645**.

As described above, all the possible connections of the selectable function computational die **600** are connected to input/output pads thus insuring a single common functional die is inventoried. The second level package provides the logic states for the option select signals **640** and will make the connections to the desired functions of the selectable function computational die **600**. The undesired functions on the selectable function computational die **600** are omitted in the mounting of the selectable function computational die from the second level package.

For discussion of a method for assembling and selecting desired options of a multiple, selectable function integrated circuit module refer to Fig. 7. A

multiple selectable function integrated circuit die is formed **700** on a

- 5 semiconductor wafer by formation and interconnection of electronic circuits on the semiconductor wafer employing known semiconductor processes.

Redistribution metal is fabricated **705** on the surface of the semiconductor wafer forming the connections of the common internal functions and the selectable internal functions of the multiple selectable function integrated circuit die to

- 10 input/output pads on the surface of the semiconductor wafer. The solder bumps are then formed and reflowed to form **710** the solder ball on the surface of the semiconductor wafer. The individual multiple selectable function integrated circuit dies are then tested **715** and the functional multiple selectable function integrated circuit dies are identified. The semiconductor wafer is then diced **720**

- 15 and the functional multiple selectable integrated circuit die are burned-in **725** to eliminate any early life failures of the functional multiple selectable function integrated circuit dies. The functional multiple selectable function integrated circuit dies are then tested **730** and the known good multiple selectable function integrated circuit die are sorted **735**, with the non-functioning die discarded. The

- 20 forming **700** of the known good multiple selectable function integrated circuit dies allows a single common design to be inventoried.

The second level package module substrate is formed **740** by applying and forming metal interconnection on substrate laminates of the second level package substrate. The laminates are bonded together to create the second level package substrate. The wiring connections on the second level package substrate may either be custom for each option selection of the multiple selectable function integrated circuit or have a common design to minimize inventory of the different option designs.

A solder mask is placed **745** on the second level package substrate. The solder mask will expose the desired interconnecting pads of the metal interconnections on the second level package substrate to implement the desired functional options of the multiple selectable function integrated circuit die. Those undesired functions have no voids in the solder mask to prevent exposure of the metal connections to prevent connection to the input/output pads of the undesired functions of the multiple selectable function integrated circuit dies. Solder paste is applied **750** to make contact with the desired interconnecting pads of the metal interconnections on the second level package substrate. The known good multiple selectable function integrated circuit die are then secured **755** to the second level package substrate to form the connections between the desired functions of the multiple selectable function integrated circuit die and external circuitry through the metal interconnections on the second level package substrate.

The second level package substrate is processed **755** through final assembly and test and is ready for further system level construction. Since the final assembly is the "gang-bonding" as in what is known in the art as "flip chip assembly", no extra cost is incurred to have the ability to select multiple functions  
5 during system and subsystem assembly.

It should be noted that the second level package substrate may be a ceramic substrate, a plastic substrate, a fiberglass reinforced substrate, a metal substrate having layers of insulative material to isolate the metal  
10 interconnections, semiconductor substrates, a glass substrate, or an integrated circuit die to form a chip-on-chip structure.

Fig. 8 illustrates a packaging structure **800** where more than one multiple selectable function integrated circuit die **805** and **810** are connected together to  
15 form a more complex subsystem having selectable interconnecting functions. The multiple selectable function integrated circuit die **805** and **810** are structured as described in Fig. 3. The selectable functions of the first multiple selectable function integrated circuit die **805** differ from those of the second multiple selectable function integrated circuit die **810**.

The selectable input functions and selectable output functions of Fig. 3 are represented jointly as the selectable input/output functions **805a**, **805b**, **810a**, and **810b**. Certain selectable input/output functions **805a** and **810a** are

connected through the selectable input/output function connectors **825** and **840** to circuitry external to the illustrated packaging structure **800**. Other selectable input/output functions **805b** and **810b** are appropriately interconnected through the selectable input/output connectors **815**.

5

The common functions **805c** and **810c** are connected to the circuitry external to the illustrated packaging structure **800** through the common function connectors **830** and **845**. The common functions **805c** of the first multiple selectable function integrated circuit die **805** are interconnected through the common function connectors **820** to the common functions **810c** of the second multiple selectable function integrated circuit die **810**.

10

The option select signals **835** and **850** are each an aggregate of the option select signals of Fig. 3. The option select signals **835** are connected to the option selector **805d** of the first multiple selectable function integrated circuit die **805**, and the option select signals **850** are connected to the option selector **810d** of the second multiple selectable function integrated circuit die **810**.

15

As described for an individual multiple selectable function integrated circuit die of Fig. 3, the selectable input/output functions **805a**, **805b**, **810a**, and **810b** are chosen by application of the appropriate logic state to the option selectors **805d** and **810d**. This is accomplished by selectively connecting or omitting connections of the option select signals **835** and **850** respectively to the options

20



selectors **805d** and **810d**. Further, those desired selectable input/output connectors **815**, **825**, and **840** are established during the attaching of the first and second multiple selectable function integrated circuit die **805** and **810** to a second level package assembly. The undesired selectable input/output

5 connectors **815**, **825**, and **840** are omitted during the attaching as described above.

The first and second multiple selectable function integrated circuit die **805** and **810** may each be a DRAM, a computational processor (microprocessor, a

10 microcontroller, a digital signal processor, etc.), or other logic or analog functional integrated circuit die. Additionally, the first multiple selectable function integrated circuit die **805** may be attached to the second multiple selectable function integrated circuit die **810**. Conversely, the second multiple selectable function integrated circuit die **810** may be attached to the first multiple selectable function

15 integrated circuit die **805**. Further, the first multiple selectable function integrated circuit die **805** and the second multiple selectable function integrated circuit die **810** may mounted one to another in a "chip-on-chip" structure. An example of the above would be the mounting of a DRAM known good integrated circuit die as the first multiple selectable function integrated circuit die **805** to a complex

20 logic function as the second multiple selectable function integrated circuit die **810**.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

5

The invention claimed is:

1. An integrated circuit module comprising:

at least one known good integrated circuit die having multiple  
selectable input functions, multiple selectable output functions,  
common functions, a function selector, all interconnected and  
connected to input/output pads;

a second level substrate onto which the known good integrated  
circuit die is mounted having connections to the input/output  
pads of the known good integrated circuit die to select desired  
selectable input functions and output functions and provide  
signal paths to transfer signals to the desired selectable input  
function and signals from the desired selectable input function  
and signals to and from the common functions, wiring  
connections between the connections to the input/output pads  
and external circuitry whereby appropriate logic states are  
applied to input/output pads connected to the function selector  
to select the desired selectable input functions and desired  
selectable input functions to configure a functional operation of  
said integrated circuit module; and

pins connected to the second level substrate to provide physical and electrical connections between the external circuitry and the wiring connections on the second level substrate.

- 5    2.    The integrated circuit module of claim 1 wherein the known good die is a DRAM having a plurality of selectable input/output organizations, whereby each of the selectable input/output organizations is selected as one of the logic states to the output function selector and connections from the second level substrate to unused output function connected to input/output pads of the DRAM are omitted from the second level substrate.
- 10
3.    The integrated circuit module of claim 1 wherein the known good die is a computational processor.
- 15    4.    The integrated circuit module of claim 3 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.
- 20    5.    The integrated circuit module of claim 1 wherein the input/output pads of the known good integrated circuit die are created during processing of a semiconductor wafer one to which the known good integrated circuit die is formed.

6. The integrated circuit of claim 1 wherein the input/output pads are gang-bonded to the second level substrate.

5 7. The integrated circuit of claim 1 wherein the known good integrated circuit die is attached to the second level substrate by a flip chip assembly.

8. The integrated circuit module of claim 1 wherein the input/output pads of the known good die have solder bumps and are arranged as a ball grid array.

9. The integrated circuit module of claim 1 wherein the second level substrate is selected from the group of substrates consisting of plastic substrates, fiberglass reinforced plastic substrates, ceramic substrates, insulator coated metal substrate, semiconductor integrated circuit die, and glass substrates.

10. The integrated circuit of claim 1 wherein in the second level substrate is a known good integrated circuit die of a second type on to which the known good integrated circuit die is mounted, whereby said known good integrated circuit die of the second type has multiple selectable input functions, multiple selectable output functions, common functions, a function selector, all interconnected and connected to input/output pads.

11. The integrated circuit of claim 10 wherein the known good integrated circuit die is a DRAM and the known good integrated circuit die of the second type is a computational processor.

5

12. The integrated circuit module of claim 11 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

10

13. A DRAM integrated circuit module comprising:

at least one known good DRAM die having address input pads connected to address selection circuitry, timing and control input pads connected to timing and control circuitry, an array of DRAM cells to retain digital data connected to the address selection circuitry and time and control circuitry, a plurality of input/output buffers connected to inputs and outputs of the array of DRAM cells to transfer digital data to and from said array of DRAM cells, a plurality of data transfer pads connected to input/output buffers, an option selector circuit connected to the input/output buffers to select which of the plurality of data transfer pads are to contain the digital data for transfer to and

15

20

from the array of DRAM cells, and a plurality of option select pads connected to the option selector circuit to provide appropriate logic states to the option selector circuit to select the data transfer pads;

5 a DRAM module substrate onto which the known good DRAM die is mounted having wiring connections between the address input pads, timing and control pads, the selected data transfer pads, the option select pads, and external circuitry; and  
a plurality of pins mounted to the module substrate to connect the  
10 wiring connections to the external circuitry.

14. The DRAM module of claim 13 wherein the address input pads, timing and control pads, data transfer pads, and option select pads are arranged in a ball grid array, whereby non-selected data transfer pins and appropriate  
15 option select pads are omitted from connection to the DRAM module substrate.

15. A digital processor module comprising:

at least one known good computational processor die having a

20 plurality of memory data transfer pads arranged in groups of memory data buses, a plurality of memory address transfer pads arranged in groups of memory address buses, a plurality of input/output interface data transfer pads arranged in

input/output interfaces, and a plurality of timing and control transfer pads arranged in timing and control interfaces, all connected to a computational processor to manipulate digital data transferred into said computational processor and transfer digital data from said computational processor, and a bus configurator connected to the memory data transfer pads, the memory address transfer pads, the input/output interface pads, and the timing and control transfer pads to configure the memory data buses, the memory address buses, the input/output interfaces, and the timing and control interfaces for transfer and manipulation of digital data, whereby the bus configurator is connected to bus configuration pads to provide logic states to determine the bus configuration;

a digital processor module substrate onto which the known good processor die is mounted having connections between external circuitry and the configured memory data buses, memory address buses, the input/output interface buses, and the timing and control interface bus; and

a plurality of pins mounted to the module substrate to connect the connections to the external circuitry.

16. The digital processor module of claim 15 wherein the memory data transfer pads, the memory address transfer pads, the input/output



interface data transfer pads, and the timing and control transfer pads are arranged in a ball grid array.

17. The digital processor module of claim 15 wherein the non-selected memory data transfer pads, memory address transfer pads, the input/output interface data transfer pads, timing and control transfer pads, and bus configuration pads are omitted from connection to the digital processor module.

18. The digital processor module of claim 15 wherein the memory data transfer pads, the memory address transfer pads, the input/output interface data transfer pads, timing and control transfer pads have solder bumps.

19. An integrated circuit module comprising:

at least one known good integrated circuit die of a first type having multiple selectable input functions, multiple selectable output functions, common functions, a function selector, all interconnected and connected to input/output pads;

at least one known good integrated circuit die of a second type having multiple selectable input functions, multiple selectable

output functions, common functions, a function selector, all interconnected and connected to input/output pads;

a second level substrate onto which the known good integrated circuit dies of the first and second type are mounted having connections to the input/output pads of the known good integrated circuit dies of the first and second type to select desired selectable input functions and output functions and provide signal paths to transfer signals to the desired selectable input function and signals from the desired selectable input function and signals to and from the common functions, wiring connections between the connections to the input/output pads and external circuitry whereby appropriate logic states are applied to input/output pads connected to the function selector to select the desired selectable input functions and desired selectable input functions to configure a functional operation of said integrated circuit module; and

pins connected to the second level substrate to provide physical and electrical connections between the external circuitry and the wiring connections on the second level substrate.

20. The integrated circuit module of claim 19 wherein the known good integrated circuit die of the first type is a DRAM having a plurality of selectable input/output organizations, whereby each of the selectable input/output organizations is selected as one of the logic states to the output function selector and connections from the second level substrate to unused output function connected to input/output pads of the DRAM are omitted from the second level substrate.
21. The integrated circuit module of claim 19 wherein the known good integrated circuit die of the second type is a computational processor.
22. The integrated circuit module of claim 21 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.
23. The integrated circuit module of claim 19 wherein the known good integrated circuit die of the second type is a DRAM having a plurality of selectable input/output organizations, whereby each of the selectable input/output organizations is selected as one of the logic states to the output function selector and connections from the second level substrate to unused output function connected to input/output pads of the DRAM are omitted from the second level substrate.

24. The integrated circuit module of claim 19 wherein the known good integrated circuit die of the first type is a computational processor.

5 25. The integrated circuit module of claim 23 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

10 26. The integrated circuit module of claim 19 wherein the input/output pads of the known good integrated circuit dies of the first and second types are created during processing of a semiconductor wafer one to which the known good integrated circuit die is formed.

15 27. The integrated circuit of claim 19 wherein the input/output pads are gang-bonded to the second level substrate.

20 28. The integrated circuit of claim 19 wherein the known good integrated circuit dies of the first and second types are attached to the second level substrate by a flip chip assembly.

29. The integrated circuit module of claim 19 wherein the input/output pads of the known good integrated circuit dies of the first and second types have solder bumps and are arranged as a ball grid array.

5 30. The integrated circuit module of claim 19 wherein the second level substrate is selected from the group of substrates consisting of plastic substrates, fiberglass reinforced plastic substrates, ceramic substrates, insulator coated metal substrate, semiconductor substrate, glass substrates, and an integrated circuit die forming a chip-on-chip structure.

10 31. A method to form an integrated circuit module comprising the steps of:  
forming a known good integrated circuit die having multiple  
selectable input functions, multiple selectable output functions,  
common functions, a selector function by the steps of;  
15 forming electronic components on a surface of a  
semiconductor wafer to form the multiple selectable input  
functions, the multiple selectable output functions,  
common functions, and the selector function,  
forming redistribution metallurgy on the surface of the  
20 semiconductor wafer to form input/output pads connected  
to the multiple selectable input functions, the multiple  
selectable output functions, the common functions, and  
the selector functions,

testing said integrated circuit die to functional integrated  
circuits die,

dicing said semiconductor wafer to circuit die, and

sorting said known good integrated circuit die; and

5 forming a second level substrate by the steps of:

forming metal interconnections on all levels of the second

level substrate, and laminating of the levels of the second

level substrate, and

applying a solder mask to a component level of said second

10 level substrate in locations to expose the input/output

pads of the common functions, desired functions of the

multiple selectable input functions and the multiple

selectable output functions, and the input/output pads to

select the desired functions with input and output selector

15 functions;

applying a solder paste to the input/output pads exposed by the

solder mask,

placing and securing the known good integrated circuit die to said

component level; and

20 performing final assembly and test of said integrated circuit module.

32. The method of claim 31 further comprising applying solder bumps to the  
input/output pads.

33. The method of claim 31 further comprising, subsequent to dicing said semiconductor substrate, burning in said functional integrated circuit die.

5 34. The method of claim 31 further comprising testing of functional integrated circuit die subsequent to dicing to determine said known good integrated circuit die.

10 35. The method of claim 31 further comprising arranging the input/output pads as a ball grid array.

15 36. The method of claim 31 wherein the known good integrated circuit die is selected from a group of integrated circuit dies consisting of DRAM dies, digital signal processor dies, microcontroller dies, microprocessor dies, and digital logic arrays.

20 37. The method of claim 31 further comprising omitting non-desired functions of the multiple selectable input functions, the multiple selectable output functions, the input selector function and output selector function by omitting coating of the input/output pads of said non-desired functions with the solder paste.

38. An input/output integrated circuit connection system to physically and electrically secure a known good integrated circuit die to a second level substrate, whereby the known good integrated circuit die has multiple selectable input functions, multiple selectable output functions, multiple common functions, input function selectors and output function selectors, whereby said input/output integrated circuit connection system comprises:

a plurality of input/output pads formed as a redistribution metal layer on a top surface of said known good integrated circuit die and arranged in rows and columns to form an array; and  
a plurality of solder balls placed on the input/output pads; and  
a solder mask placed on a component surface of the second level substrate, having voids to allow connections of the solder balls of the input/output pads of the common functions, and desired multiple selectable input functions, desired multiple selectable output functions, desired connections of the input function selector, and desired connections of the output function selector to wiring contacts on the second level substrate, and no voids to prevent connection of the solder balls of undesired function and undesired connections to the input and output function selectors.



39. The input/output integrated circuit connection system of claim 38 wherein the wiring contacts on the second level substrate are connected to external circuitry.

5 40. The input/output integrated circuit connection system of claim 38 wherein the second level substrate is selected from the group of substrates consisting of plastic substrates, fiberglass reinforced plastic substrates, ceramic substrates, insulator coated metal substrate, semiconductor substrates, glass substrates, and integrated circuit substrates to for a chip-on-chip structure.

10 41. The input/output integrated circuit connection system of claim 38 wherein the known good integrated circuit die is a DRAM and the multiple selectable input and output functions are the number of bits to be transferred into and out of said DRAM.

15 42. The input/output integrated circuit connection system of claim 38 wherein the known good integrated circuit die is a computational processor.

20 43. The integrated circuit module of claim 42 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

44. The input/output integrated circuit connection system of claim 38 wherein the desired connections and the undesired connections of the function selector create logic states at the inputs of said function selector to choose the desired input functions and the desired output functions.

45. A method to form integrated circuit connections to physically and electrically connect a known good integrated circuit die to a second level substrate, whereby the known good integrated circuit die comprises multiple selectable input functions, multiple selectable output functions, multiple function selectors, and whereby said method comprises the steps of:

forming a plurality of input/output pads of a redistribution metal on a top surface of said known good integrated circuit die;

arranging said input/output pads in rows and columns

forming solder bumps on said input/output pads;

placing a solder mask on a component surface of the second level substrate, having voids to allow connections of the solder balls of the input/output pads of the common functions, and desired multiple selectable input functions, desired multiple selectable output functions, desired connections of the function selector to wiring contacts on the second level substrate, and no voids to

prevent connection of the solder balls of undesired function and  
undesired connections to the function selectors; and  
melting said solder bumps to make connections between said  
known good integrated circuit die and signal path within said  
5 second level substrate.

46. The method of claim 45 wherein said wiring paths on the second level  
substrate interconnect the known good integrated circuit die with external  
circuitry.

47. The method of claim 45 wherein the second level substrate is selected  
from the group of substrates consisting of plastic substrates, fiberglass  
reinforced plastic substrates, ceramic substrates, insulator coated metal  
substrate, semiconductor substrates, glass substrates, and an integrated  
15 circuit die to form a chip-on-chip structure.

48. The method of claim 45 wherein the known good integrated circuit die is a  
DRAM and the multiple selectable input and output functions are the  
number of bits to be transferred into and out of said DRAM.

49. The method of claim 45 wherein the known good integrated circuit die is a  
computational processor.

50. The integrated circuit module of claim 49 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

5

51. The method of claim 45 wherein the desired connections and the undesired connections of the function selector create logic states at the inputs of said function selector to choose the desired input functions and the desired output functions.

10

### Abstract

An integrated circuit module has a common function known good integrated circuit die with selectable functions. The selectable functions are selected during packaging of the known good integrated circuit die. The known good integrated circuit die is mounted to a second level substrate. The second level substrate has wiring connections to the input/output pads of the known good integrated circuit die that select desired input functions and output functions. Further, the wiring connections on the second level substrate provide signal paths to transfer signals to the desired input function and signals from the desired output function, and signals to and from the common functions. Also, the wiring connections form connections between the input/output pads and external circuitry. To select the desired input functions and the desired output functions, appropriate logic states are applied to input/output pads connected to a function selector to configure a functional operation of the integrated circuit module. The second level module substrate has connector pins to provide physical and electrical connections between the external circuitry and the wiring connections on the second level substrate.

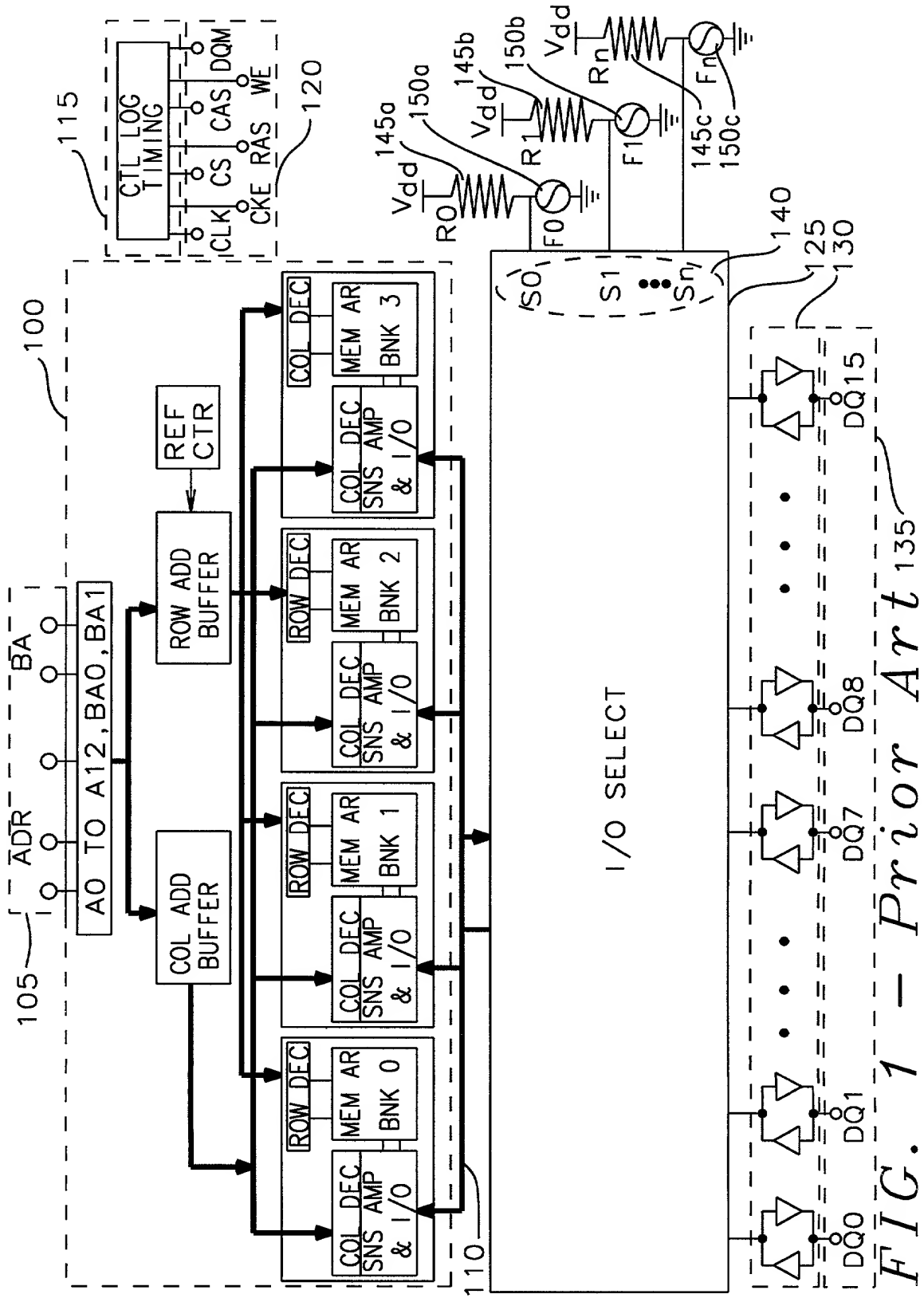
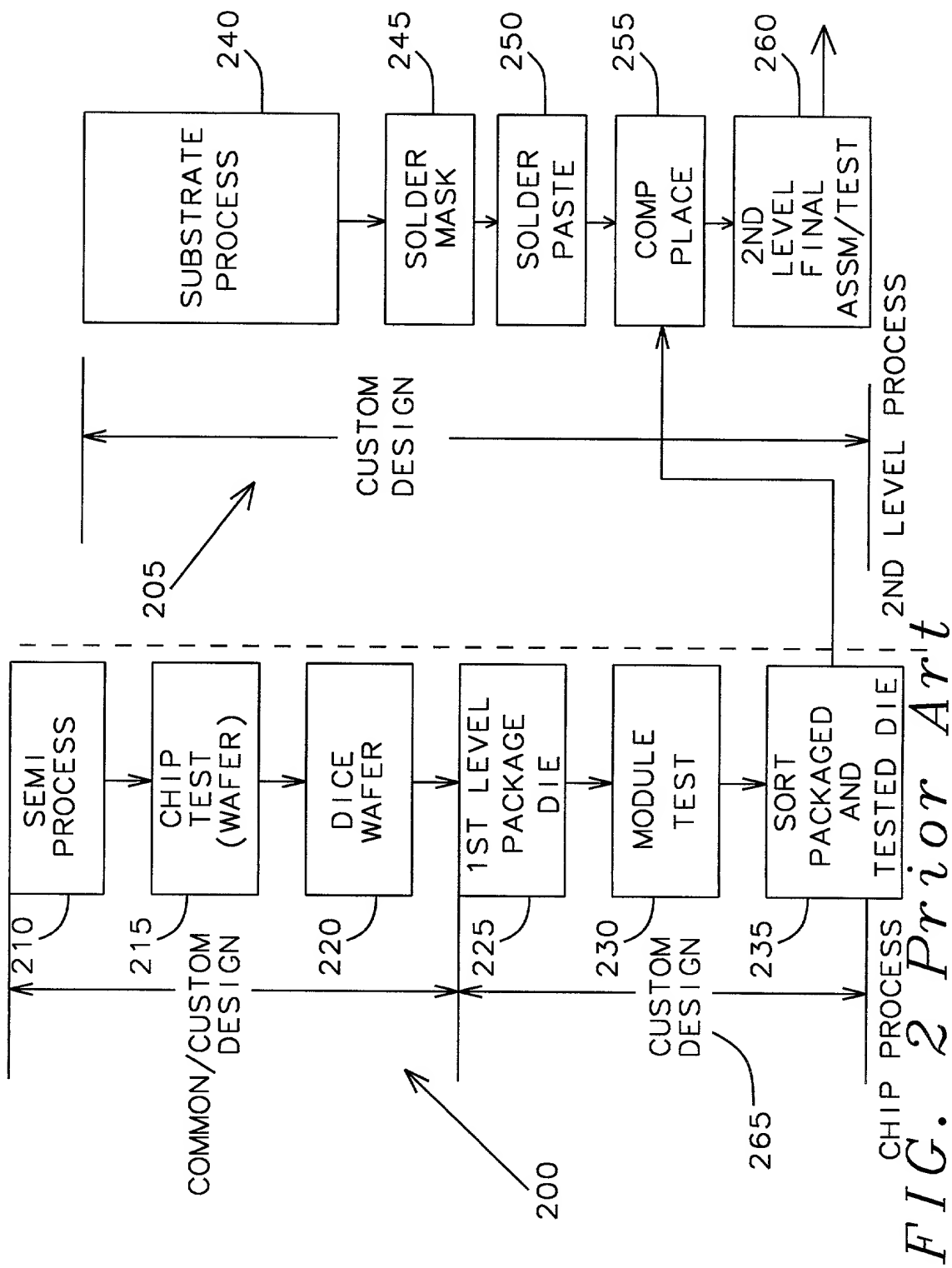


FIG. 1 - Prior Art







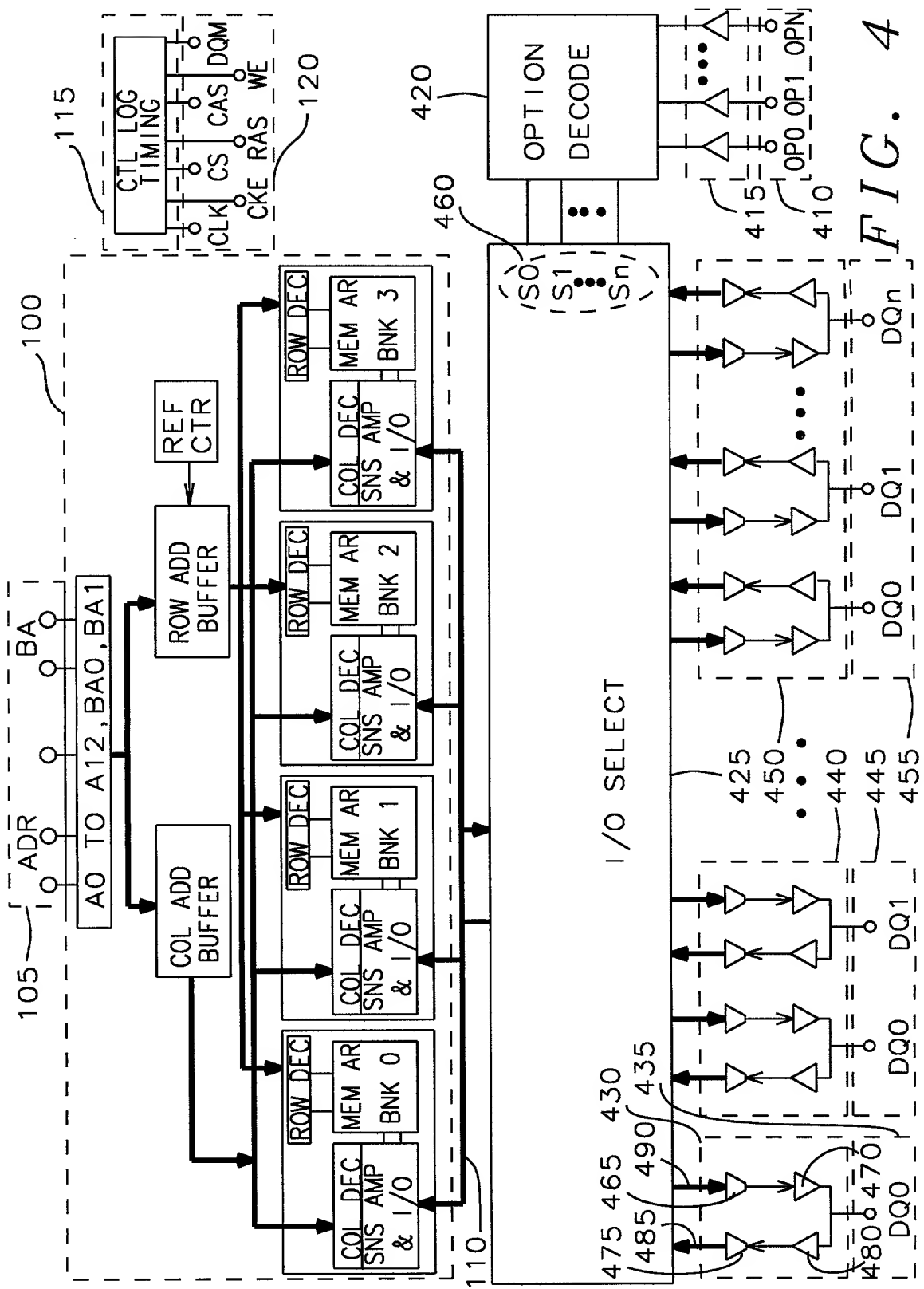


FIG. 4

FIG. 5a

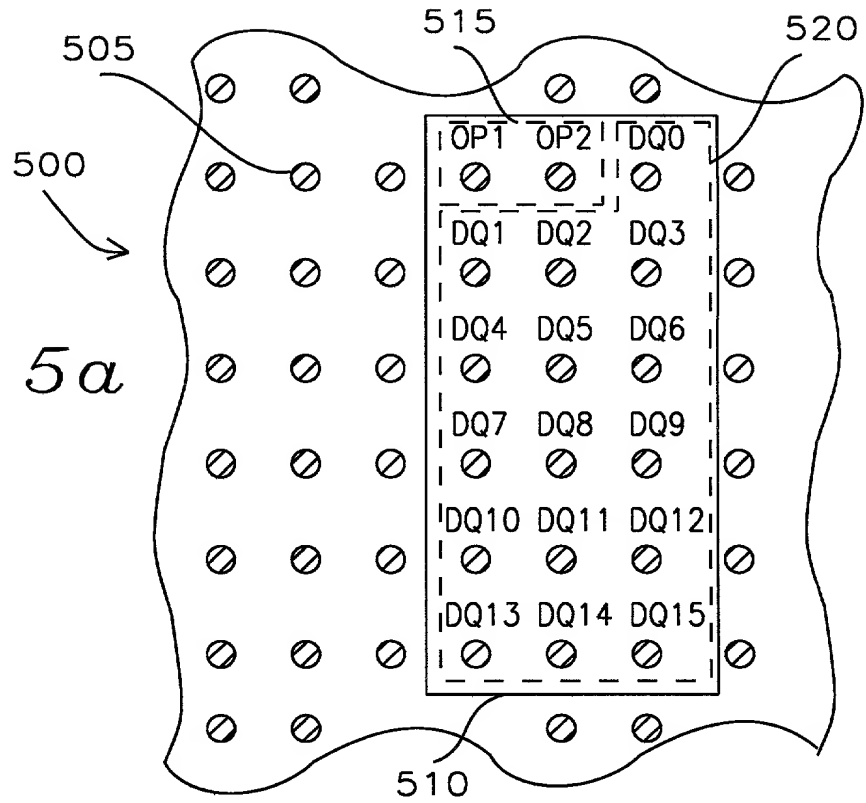


FIG. 5b

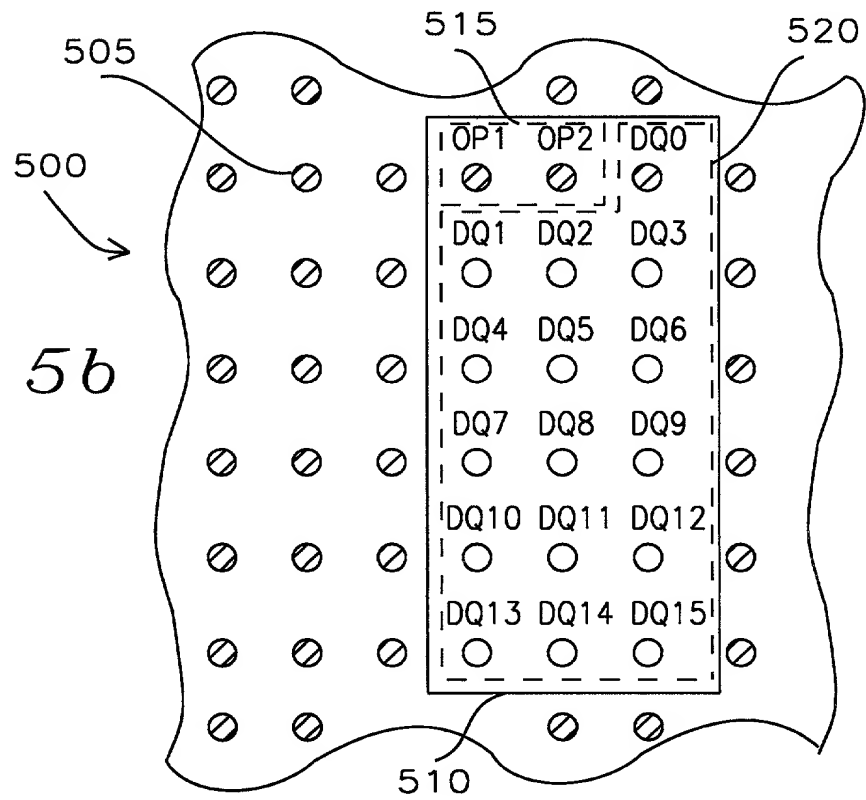


FIG. 5c

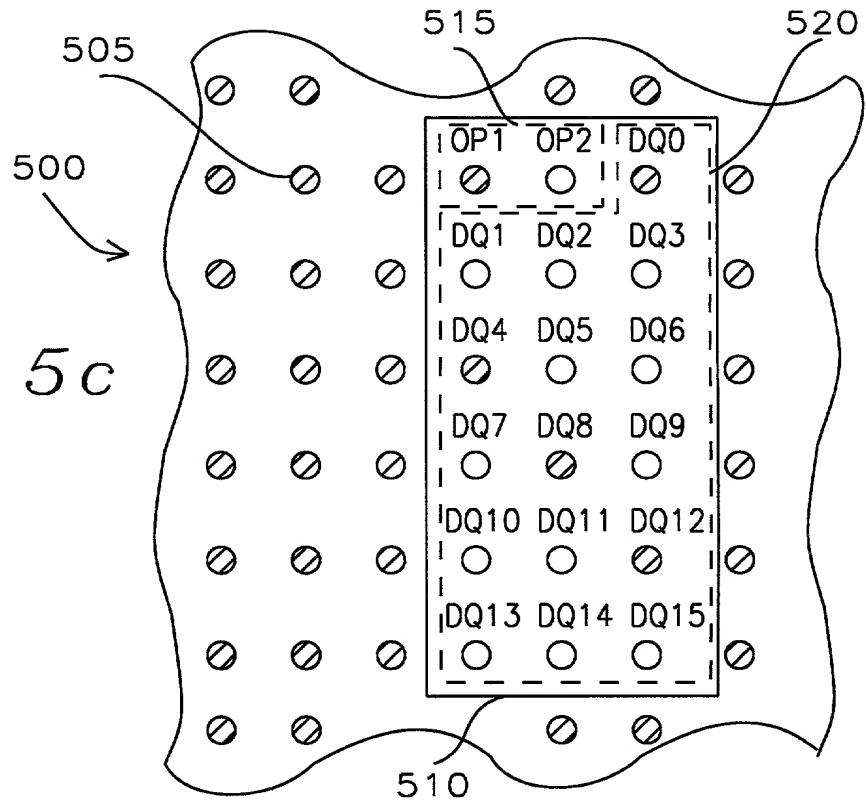


FIG. 5d

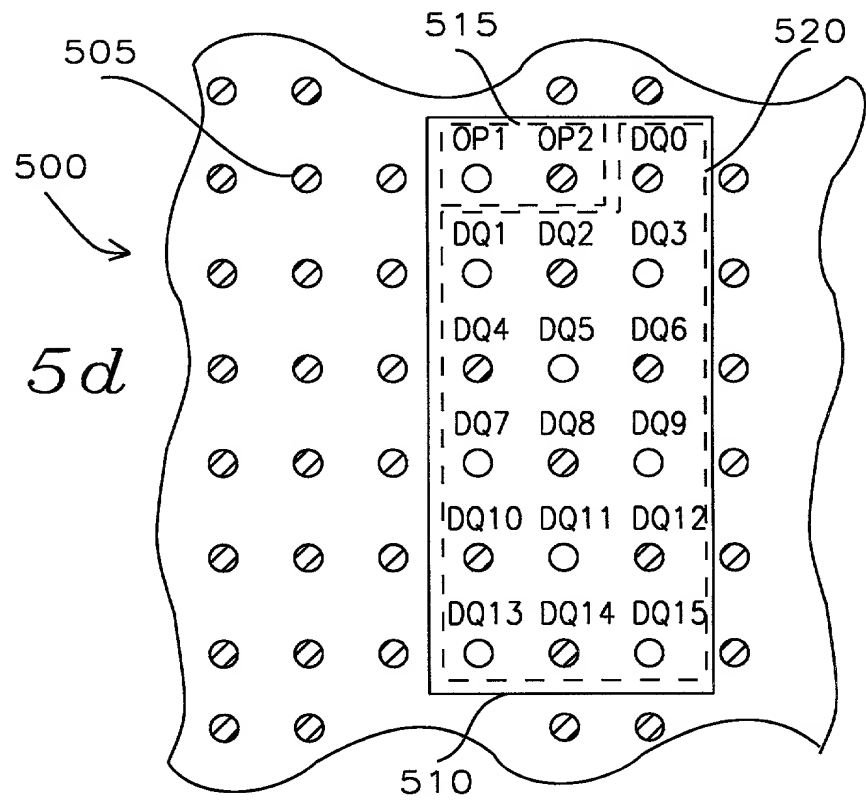
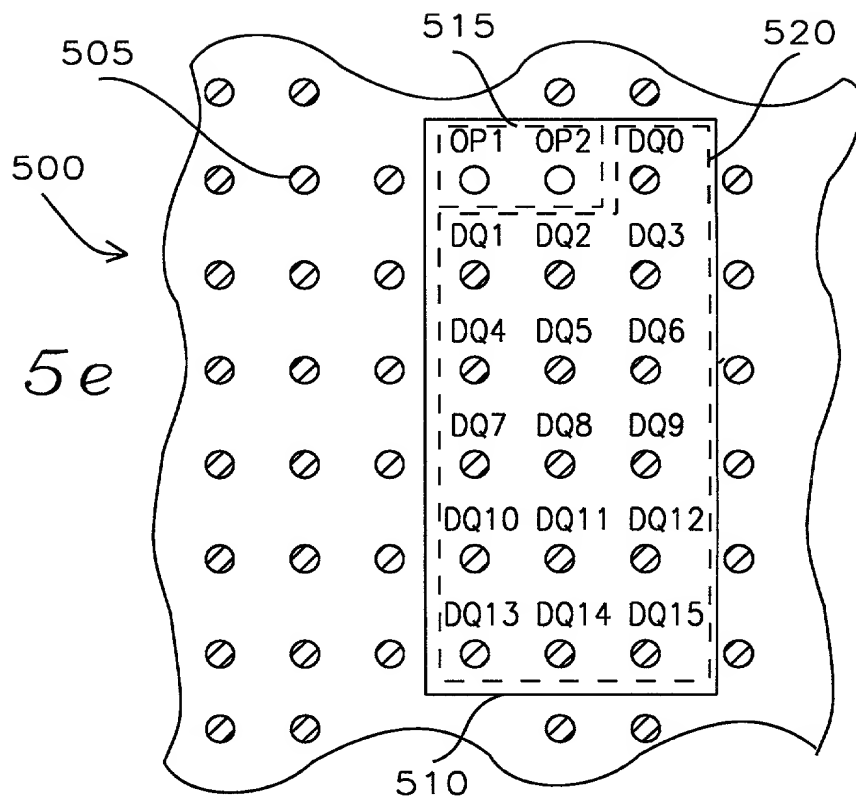


FIG. 5e



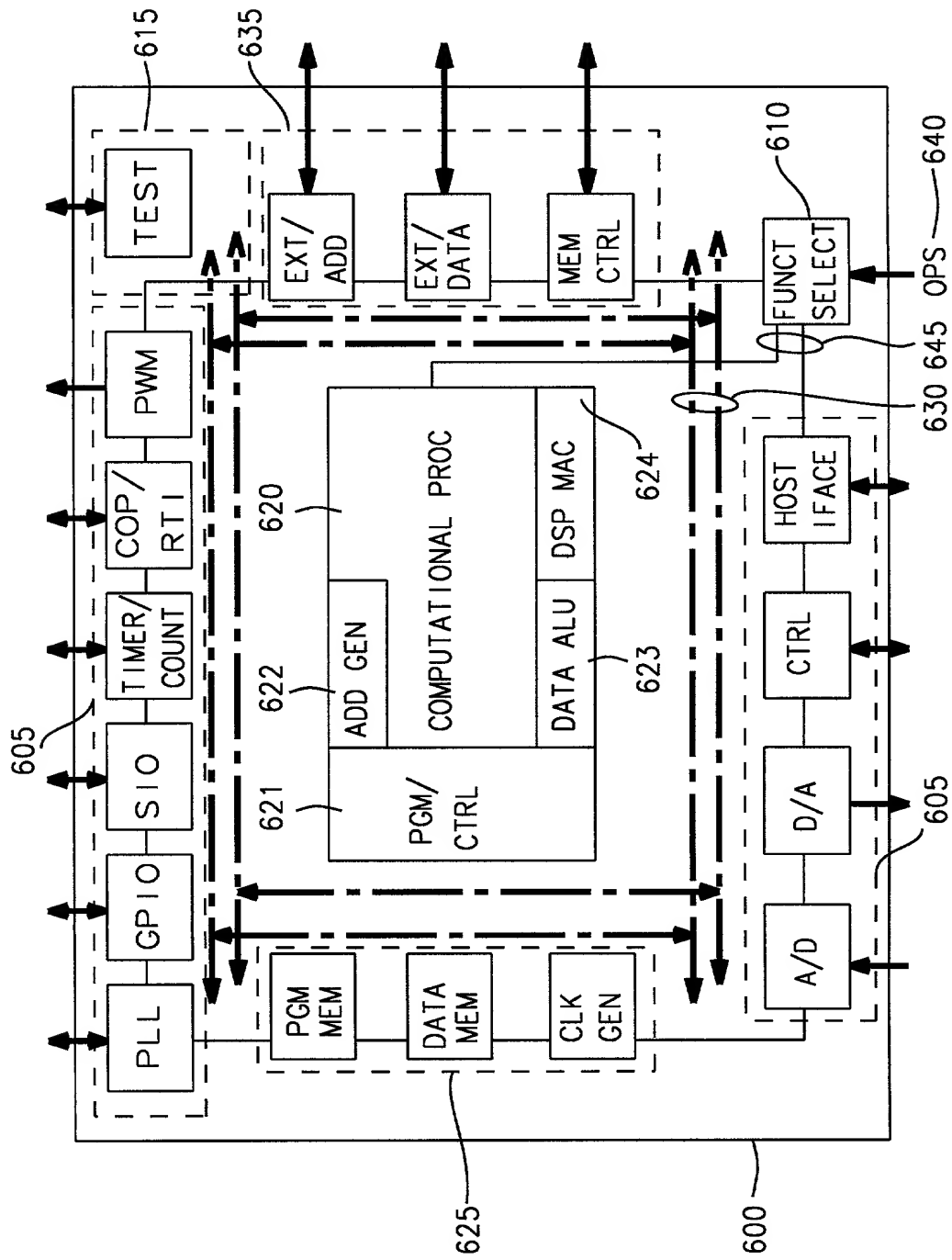


FIG. 6

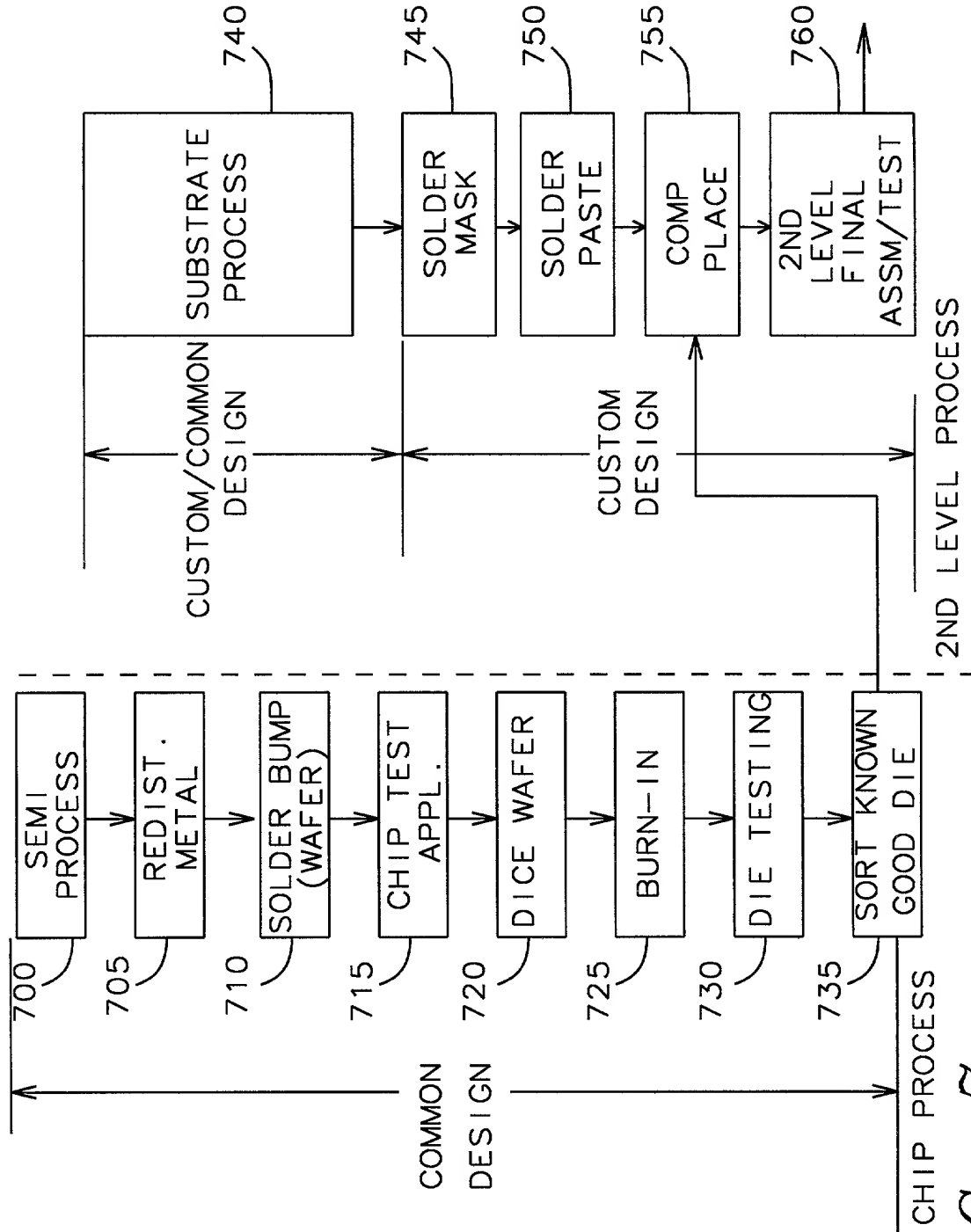


FIG. 7

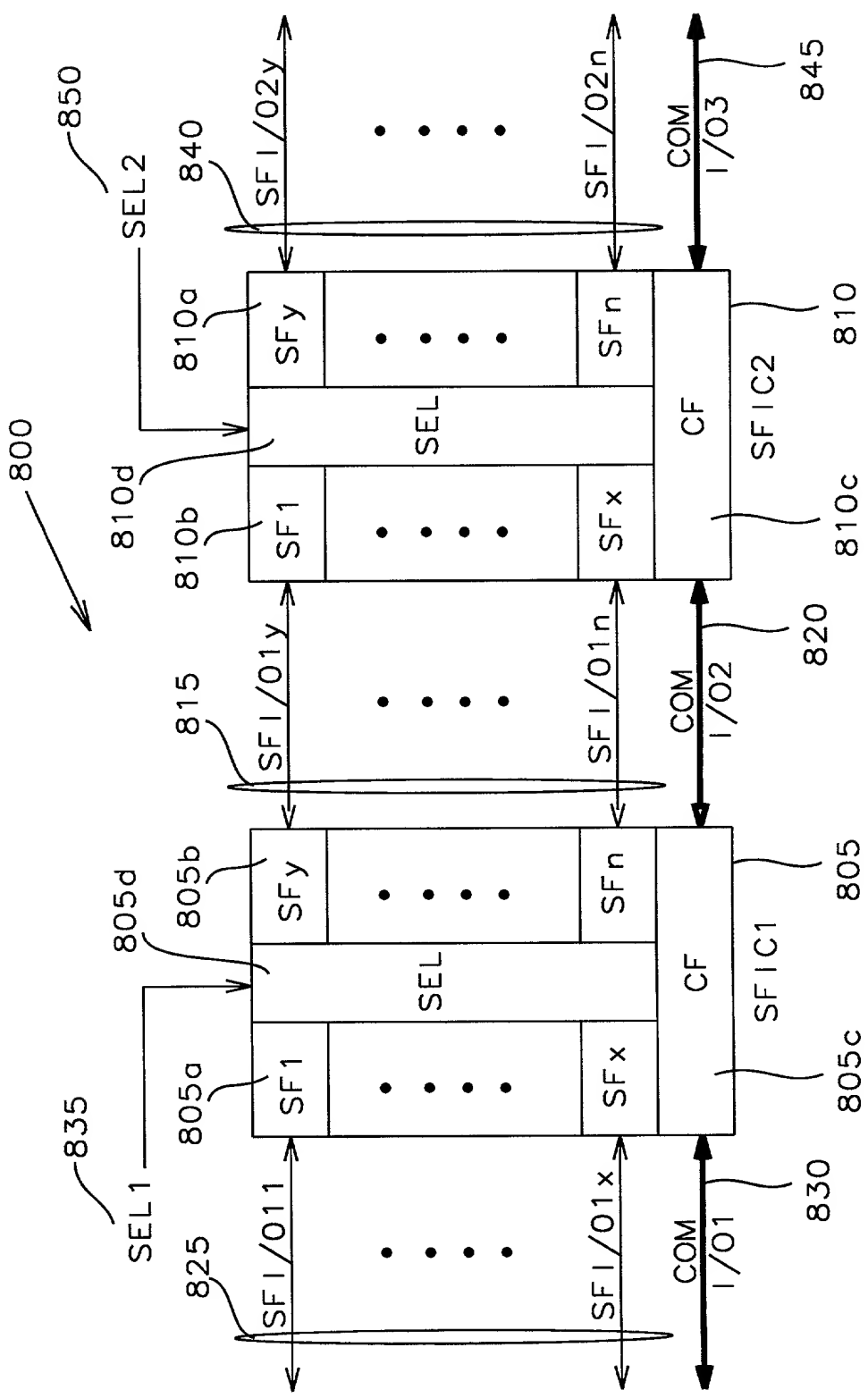


FIG. 8

# DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

DOCKET NO. MSLIN98-005

As a below named Inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A Multiple Selectable Function Integrated Circuit Module  
the specification of which (check one)

X is attached hereto.

was filed on \_\_\_\_\_

Application Serial No \_\_\_\_\_

and was amended on \_\_\_\_\_

(if applicable)

I hereby state that I have reviewed and understand the contents of the above Identified specification including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed:

(Number)	(Country)	(Day/Month/Year Filed)
----------	-----------	------------------------

(Number)	(Country)	(Day/Month/Year Filed)
----------	-----------	------------------------

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
--------------------------	---------------	---

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**POWER OF ATTORNEY.** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name & registration no.)

GEORGE O. SAILE. (Reg. No. 19,572), STEPHEN B. ACKERMAN (Reg. No. 37,761)

Send Correspondence to: 20 MCINTOSH DRIVE, POUGHKEEPSIE, NEW YORK 12603

Direct telephone Calls to: (name & telephone number) GEORGE O. SAILE NEW YORK 914 452 5863

MOU-SHIUNG LIN

Full name of sole or first inventor

Date

Mou-Shiung Lin  
Inventor's Signature

January 24, 1999

24 Bamboo 3rd Rd. 6F, Hsinchu, Taiwan  
Residence

U.S.  
Citizenship

24 Bamboo 3rd Rd. 6F, Hsinchu, Taiwan  
Post Office Address



**STATEMENT CLAIMING SMALL ENTITY STATUS  
(37 CFR 1.9(f) & 1.27(b))--INDEPENDENT INVENTOR**

Docket Number (Optional)

MSLIN 98-005

Applicant, Patentee, or Identifier: MOU-SHIUNG LIN

Application or Patent No. \_\_\_\_\_

Filed or Issued: \_\_\_\_\_

Title: A Multiple Selectable Function Integrated  
Circuit Module

As a below named inventor, I hereby state that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees to the Patent and Trademark Office described in:

- ☒ the specification filed herewith with title as listed above.  
☐ the application identified above.  
☐ the patent identified above.

I have not assigned, granted, conveyed, or licensed, and am under no obligation under contract or law to assign, grant, convey, or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e)

Each person, concern, or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

- ☒ No such person, concern, or organization exists.  
☐ Each such person, concern, or organization is listed below.

Separate statements are required from each named person, concern, or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

MOU-SHIUNG LIN

NAME OF INVENTOR

NAME OF INVENTOR

NAME OF INVENTOR

Mou-Shiung Lin

Signature of Inventor

Signature of inventor

Signature of Inventor

January 25, 1999

Date

Date

Date